CLAIMS

WHAT IS CLAIMED:

1. A built-in self-test controller, comprising:

a logic built-in self-test engine capable of executing a logic built-in self-test, including:

a logic built-in self-test state machine; and

a pattern generator seeded with a first primitive polynomial; and

a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial.

2. The built-in self-test controller of claim 1, wherein the first primitive polynomial is $x^{31} + x^3 + 1$.

3. The built-in self-test controller of claim 1, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.

4. The built-in self-test controller of claim 1, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

5. The built-in self-test controller of claim 1, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

6. The built-in self-test controller of claim 1, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done;

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

7. The built-in self-test controller of claim 1, wherein the seed for the pattern generator is externally configurable.

8. A built-in self-test controller, comprising:

means for executing a logic built-in self-test, including a pattern generator seeded with a first primitive polynomial; and

means for storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial.

9. The built-in self-test controller of claim 8, wherein the first primitive polynomial is $x^{31} + x^{3} + 1$.

10. The built-in self-test controller of claim 8, wherein the second primitive polynomial is $x^{32} + x^{28} + x + 1$.

11. The built-in self-test controller of claim 8, wherein the seed for the pattern generator is externally configurable.

12. A integrated circuit device, comprising:

a plurality of memory components;

a logic core;

a testing interface; and

a built-in self-test controller, including:

a logic built-in self-test engine capable of executing a logic built-in self-test and storing the results thereof, including:

a logic built-in self-test state machine; and

a pattern generator seeded with a first primitive polynomial; and a multiple input signature register capable of storing the results of an executed logic built-in self-test, the contents thereof being stored per a second primitive polynomial.

13. The integrated circuit device of claim 12, wherein the first primitive polynomial is $x^{31} + x^{3} + 1$.

14. The integrated circuit device of claim 12, wherein the first primitive polynomial is $x^{32} + x^{28} + x + 1$.

15. The integrated circuit device of claim 12, wherein the logic built-in self-test state machine further comprises:

a reset state entered upon receipt of an external reset signal;

an initiate state entered from the reset state upon receipt of a logic built-in self-test run signal;

a scan state entered from the initiate state upon the initialization of components and signals in the logic built-in self-test domain in the initiate state;

a step state entered into from the scan state and from which the scan state is entered unless the content of the pattern generator equals a predetermined vector count; and

a done state entered into when the content of the pattern generator equals the predetermined vector count.

16. The integrated circuit device of claim 12, wherein the pattern generator comprises a linear feedback shift register seeded with a primitive polynomial.

17. The integrated circuit device of claim 12, wherein the multiple input signature register includes at least one of:

a bit indicating whether the logic built-in self-test is done;

a bit indicating an error condition arose; and

a bit indicating whether the stored results are from a previous logic built-in self-test run.

18. The integrated circuit device of claim 12, further comprising:

a memory built-in self-test engine; and

a memory built-in self-test signature register capable of storing the results of the memory built-in self-test.

19. The integrated circuit device of claim 12, wherein the memory components include a static random access memory device.

20. The integrated circuit device of claim 12, wherein testing interface comprises a Joint Test Action Group tap controller.

21. The integrated circuit device of claim 12, wherein the seed for the pattern generator is externally configurable.

22. A method for performing a logic built-in self-test, the method comprising:

seeding a pattern generator in a logic built-in self-test engine with a first polynomial;

executing a logic built-in self-test using the contents of the pattern generator; and

storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial.

23. The method of claim 22, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^3 + 1$.

24. The method of claim 23, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is $x^{32} + x^{28} + x + 1$.

25. The method of claim 22, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is $x^{32} + x^{28} + x + 1$.

26. The method of claim 22, wherein executing the logic built-in self-test includes:

initiating a plurality of components and signals in a logic built-in self-test domain of the dual mode built-in self-test controller upon receipt of a logic built-in self-test run signal;

scanning a scan chain upon the initialization of the components and the signals;

stepping to a new scan chain; and

repeating the previous scanning and stepping until the content of the pattern generator equals a predetermined vector count.

27. The method of claim 26, further comprising at least one of:.

setting a bit in a multiple input signature register indicating whether the logic built-in self-test is done;

setting a bit in the multiple input signature register indicating an error condition arose; and

setting a bit in the multiple input signature register indicating whether the stored results are from a previous logic built-in self-test run.

28. The method of claim 22, further comprising externally configuring the seed.

29. A method for testing an integrated circuit device, the method comprising:

interfacing the integrated circuit device with a tester;

performing a logic built-in self-test, including:

seeding a pattern generator in a logic built-in self-test engine with a first polynomial;

executing a logic built-in self-test using the contents of the pattern generator; and

storing the results of an executed logic built-in self-test in a multiple input signature register utilizing a second primitive polynomial; and

reading the stored results.

30. The method of claim 29, wherein seeding the pattern generator with the first primitive polynomial includes seeding the pattern generator with the polynomial $x^{31} + x^{3} + 1$.

31. The method of claim 29, wherein storing the results of the executed logic built-in self-test utilizing the second primitive polynomial utilizes the primitive polynomial is $x^{32} + x^{28} + x + 1$.

32. The method of claim 29, further comprising externally configuring the seed.

33. The method of claim 29, further comprising performing a memory built-in self-test.